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10/648,086	08/26/2003	Sung-Ryul Kim	5649-1064	2755

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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,086	KIM ET AL.	
	Examiner	Art Unit	
	John P. Trimmings	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/26/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *2-10,12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/26/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-14 are presented for examination.

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Korea on 8/29/2002. It is noted, however, that applicant has not filed a certified copy of the English language translation of the application as required by 35 U.S.C. 119(b).

2. Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a translation of the foreign application should be submitted under 37 CFR 1.55 in reply to this action.

Claim Objections

3. Claims 2-10 and 12-14 are objected to because of the following informalities: In the interest of clarity, the examiner requests the applicant to replace the first word of each claim ("A") with the word, "The", because it is not clear that each dependent claim relies on the independent claim (1 or 11). Appropriate correction is required.

4. Claim 3 is objected to because of the following informalities:

The 4th line should be corrected to recite, "... the first externally-applied ...".

The 6th line should be corrected to recite, "... enable the subsets of ...".

5. Claim 6 is objected to because of the following informality: The examiner requests the 2nd line be corrected to recite, "... comprises ~~an~~ a write inhibit ...".

6. Claim 8 is objected to because of the following informalities:

The examiner requests the 4th line be corrected to recite, "... in response to a first state ...".

The examiner requests the 6th line be corrected to recite, "... a first of the plurality of group control signals ...", because the limitation follows claim 3.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 7-9 and 12-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention:

As per claim 7:

Claim 7 recites the limitation "the write inhibit signal buffer control circuit" in line 4. There is insufficient antecedent basis for the limitation in the claim.

As per claim 8:

Claim 8 recites the limitation "a first write inhibit buffer enable signal" in line 1, but the examiner is not sure if the limitation refers to claim 7 or to a new instantiation of a

signal. Also, line 6 recites, "a first group control signal", and the examiner is also unsure if the limitation refers to claim 4 or to a new instantiation of a signal. And line 7 recites, "the first write inhibit signal buffer control signal", but the examiner is not sure if the applicant really means, "the first write inhibit signal buffer enable signal". Therefore the claim is indefinite.

As per claim 9:

Claim 9 recites the limitation "a output control signal" in line 4, but the examiner is not sure if the limitation refers to claim 4 or to a new instantiation of a new signal. Therefore the claim is indefinite. Also, line 7 recites, "an input/output pin", but the examiner is not sure if the limitation refers to claim 1 or to a new instantiation of a new signal. Therefore the claim is indefinite.

Claim 9 recites the limitation "the external clock" in line 5. There is insufficient antecedent basis for the limitation in the claim.

As per claim 12:

Line 2 recites, "data input/output pins", but the examiner is not sure if the limitation refers to claim 11 or to a new instantiation of a new signal. Also, according to the drawings, the applicant invention connects input/output pins that are common to external data lines. But the claim restricts the input/output pins to an external data line, and so the claim is indefinite because it reads different than the drawings and the Disclosure state. For the same reason, the word "line" in line 6 is also indefinite.

As per claim 13:

Line 2 of the claim is indefinite because it specifies "the external data line", but the examiner believes that it should be lines.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-7 and 11-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Muhmenthaler et al. (herein Muhmenthaler), U.S. Patent No. 5293386.

As per claims 1 and 11:

Muhmenthaler teaches a memory device and method based on the device (see Title), comprising: a plurality of data output circuits (FIG. 2 GPIO), respective ones of which are configured to receive data from respective internal data lines (FIG. 2 GPDB) and respective ones of which are coupled to respective data input/output pins (FIG. 2 101, 102); and a data output control circuit (FIG. 2 CONTROL) operative to selectively enable subsets of the plurality of data output circuits (FIG. 2 GPAD) to drive their respective corresponding data input/output pins responsive to an externally-applied control signal (FIG. 2 ACR, /RAS, etc).

As per claims 2 and 13:

Muhmenthaler further teaches the memory device/method according to claim 1, wherein the data output control circuit is operative to selectively cause subsets of the plurality of data output circuits to present a high impedance at their respective corresponding data input/output pins (column 17 lines 43-45).

As per claim 3:

Muhmenthaler further teaches the memory device according to claim 1, wherein the data output control circuit comprises: a command decoder (FIG. 2 CONTROL) operative to generate test mode command signals and read command signals responsive to first externally-applied control signals (FIG. 2 TEST, RD responsive to R/W, ACR, RAS, CAS); and a data output selection circuit (FIG. 2 MAIO) coupled to the command decoder and operative to selectively enable subsets of the plurality of data output circuits responsive to the test mode command signals, the read command signals, and second externally-supplied control signals (see FIG. 9).

As per claim 4:

Muhmenthaler further teaches the memory device according to claim 3: wherein the data output selection circuit comprises: a data output controller circuit (FIG. 9 MACTRL) configured to receive a plurality of group control signals (FIG. 9 IOAD) and operative to generate respective output control signals (FIG. 9 MAADRD, MAADWR) responsive to respective ones of the group control signals; and a plurality of write inhibit signal input buffer circuits (FIG. 9 MAWR, MARD), respective ones of which are configured to receive respective ones of a plurality of externally-applied write inhibit signals (FIG. 9 MAADRD, MAADWR) and operative to generate respective ones of the

group control signals therefrom (FIG. 9 $MAWR_{P,I}$ for example); and wherein respective subsets of the plurality of data output circuits (FIG. 11 for example) are configured to receive respective ones of the output control signals (FIG. 11 $MAARD_I$) and are operative to be enabled and disabled responsive thereto (FIG. 11 $MARD_{P,I}$).

As per claim 5:

Muhmenthaler further teaches the memory device according to claim 4, wherein the data output controller circuit comprises: a first data output controller circuit (FIG. 9 MACTRL) that applies an enable signal to all of the plurality of data output circuits (FIG. 9 MAADRD) responsive to a read command signal generated by the command decoder (FIG. 9 MAADRD); a second data output controller circuit (FIG. 9 MAWR) that receives a first group control signal (FIG. 9 $MAWR_{I1..R}$) and that generates a first group enable signal for a first subset of the plurality of data output circuits (FIG. 9 101); and a third data output controller circuit (FIG. 9 MARD) that receives a second group control signal (FIG. 9 $MARD_{I..R}$) and that generates a second group enable signal for a second subset of the plurality of data output circuits (FIG. 9 102).

As per claim 6:

Muhmenthaler further teaches the memory device according to claim 4, wherein the data output control circuit further comprises an write inhibit signal input buffer control circuit (FIG. 9 MACTRL) operative to enable (FIG. 9 MAADWR, MAADRD) the plurality of write inhibit signal input buffer circuits (FIG. 9 MARD/MAWR) responsive to a test mode command signal generated by the command decoder (FIG. 2 CONTROL).

As per claim 7:

Muhmenthaler further teaches the memory device according to claim 6, wherein the write inhibit signal buffer control circuit (FIG. 9 MACTRL) further comprises: a control signal generator circuit which outputs a write inhibit signal buffer control signal (FIG. 9 MAADWR) in response to a data write command signal from the command decoder (FIG. 9 IOAD and FIG. 2 R/W); and a logic circuit that logically combines the write inhibit signal buffer control signal and the test mode signal (FIG. 10 MAADWR) and responsively applies a write inhibit signal buffer enable signal (FIG. 9 MAADWR) to the plurality of write inhibit signal input buffer circuits (FOG. 9 MAWR).

As per claim 12:

Muhmenthaler further teaches the method according to claim 11, further comprising: connecting data input/output pins (FIG. 2 101, 102) coupled to first and second data output circuits (FIG. 2 MAIO, GPIO) of respective first and second subsets of the plurality of data output circuits (FIG. 2 GPIO) in common to an external data line; and alternately enabling the first and second data output circuits (FIG. 2 GPAD) responsive to the control signal (FIG. 2 CONTROL ACR) to drive the external data line with data from first and second different internal data lines (FIG. 2 GPDB) of the memory device.

As per claim 14:

Muhmenthaler further teaches the method according to claim 12, wherein alternately enabling the first and second data output circuits responsive to the control signal to drive the external data line with data from first and second different internal

data lines of the memory device comprises: generating a test mode command signal (FIG. 2 TEST) from a command decoder (FIG. 2 CONTROL) of the memory device; enabling a plurality of write inhibit signal input buffers (FIG. 2 GPIO, MAIO) of the memory device responsive to the test mode command signal; generating a first read command signal (FIG. 2 RD) from the command decoder; transitioning a first write inhibit signal (FIG. 9 $MAADWR_{I,1..R}$) at an input of a first write inhibit buffer of the memory device (FIG. 9 MAWR); enabling the first subset of the plurality of data output circuits (FIG. 9 MAADRD) responsive to the first read command signal (FIG. 2 RD) and to the transition of the first write inhibit signal to thereby drive a set of external data lines (FIG. 9 101) with data from a first set of internal data lines (FIG. 9 $MARD_{I,1..R}$); generating a second read command signal from the command decoder (FIG. 11 TEST); transitioning a second write inhibit signal at an input of a second write inhibit buffer (FIG. 9 $MAADWR_{I,1..R}$); enabling the second subset of the plurality of data output circuits responsive to the second read command signal and to the transition of the second write inhibit signal to thereby drive the set of external data lines (FIG. 9 102) with data from a second set of internal data lines (FIG. 11 RDU2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muhmenthaler et al. (herein Muhmenthaler), U.S. Patent No. 5293386, in view of Varshney, U.S. Patent No. 4495603.

As per claim 8:

Muhmenthaler fails to further teach the memory device according to claim 7, wherein a write inhibit signal input buffer circuit (FIG. 9 MAWR, FIG. 12) of the plurality of write inhibit signal input buffer circuits (FIG. 9 MAWR, MARD) comprises: a voltage comparison circuit which, in response to first state of a first write inhibit buffer enable signal, compares a write inhibit signal to a reference voltage and outputs a first group control signal responsive to the comparison; and an output control circuit, which, in response to a second state of the first write inhibit signal buffer control signal, forces the first group control signal to a signal ground voltage. But in the analogous art of Varshney, such an arrangement is made to control the combining and separation of I/O pins during test. FIG. 7 illustrates the device which may be set or disabled by a fusible link, where the fusible V_R reference determines how the data is conducted in and out of the memory during test (V_{IN}). In column 5 lines 18-67 and column 6 lines 1-2, the operation is explained, and the advantage, being the capability to vary the end-use of the circuit but take advantage of the faster testing capabilities. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include the comparator of Varshney with the Muhmenthaler system in order to improve test times as well as end-use of the product.

As per claim 9:

Muhmenthaler further teaches the memory device according to claim 4, wherein a data output circuit (FIG. 2 GPIO/MAIO) of the plurality of data output circuits comprises: a data input/output (DQ) buffer circuit (FIG. 9 MARD) configured to receive data from an internal data line (FIG. 2 GPIO/GPDB) and a output control signal from the data output controller circuit (FIG. 9 MAADRD, MAADWR) and a driver circuit (see FIG. 11 OUTRD) that drives an input/output pin (FIG. 11 101). But Muhmenthaler fails to show the clock timing. But Varshney is operative to generate a synchronized data signal (FIG. 7 test clock TC combined with read, FIG. 6A TCR for example) synchronized to the external clock signal (FIG. 7 (V_{IN}). And in view of the motivation previously stated, the claim is rejected.

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muhmenthaler et al. (herein Muhmenthaler), U.S. Patent No. 5293386, in view of the applicant's admitted prior art in the Background (herein AAPA) of the application. The AAPA discloses a memory device according to claim 1, configured to operate as a double date rate synchronous dynamic random access memory (DDR SDRAM) (see pages 2-4 of the Background). The examiner, being one with ordinary skill in the art, at the time of the invention, would have recognized the obvious benefit of applying a modified I/O pin arrangement of Muhmenthaler during test in order to speed up a memory testing process, and that a DDR memory, as well as many other types of memories, would benefit from such a combination, therefore the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John P Trimmings
Examiner
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